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10/679,594	10/06/2003	Neil Johnson	ALT.P026	5941

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EXAMINER	
FARROKH, HASHEM	
ART UNIT	**PAPER NUMBER**
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,594	JOHNSON, NEIL	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-16 and 22* is/are rejected.

7)☒ Claim(s) *8,9 and 17-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/679,594 has a total of 22 claims pending in the application; there are 3 independent claims and 19 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by *U.S. Patent No. 6,304,936 B1 to Sherlock.*

1. *In regard to claim 16, Sherlock teaches*:

A method for managing data," **(e.g., see column 1, lines 38-42).** *For example the method comprises using multiple Logical FIFOs to manage data.*

"comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device;" **(e.g., see column 8, lines 36-48; elements 414 and 418 in Fig. 4).** *For example Sherlock teaches that that Next Read Register File (element 414) contains read pointers or addresses pointing to next data to be outputted from a logical FIFO within the Main Register File (element 414) shown in Fig. 4. The logical FIFO 3 represents the first FIFO recited in the claim.*

"preparing next data from a next storage element from the first FIFO memory for output." **(e.g., see column 8, lines 55-64).** *For example after the first data is read out*

the pointer to the next data is prepared in the Next Read Register File 414. When logical FIFO 3 is again selected, the next data from logical FIFO 3 will be outputted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock in view of U.S Patent Publication No. 2003/0115403 A1 to Bouchard et al. (hereinafter Bouchard).

2. In regard to claim 22, Sherlock teaches all limitations included in claim 16 but does not expressly teach: "writing data into the plurality of FIFO memories in a round robin fashion."

Bouchard teaches: "writing data into the plurality of FIFO memories in a round robin fashion." **(e.g., see paragraph 33 in page 3)** *for selecting the FIFO queues for the access requests in accordance to round-robin selection process.*

Disclosures by Bouchard and Sherlock are analogous since both references teach managing data using FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the teaching of Sherlock to include the round-robin FIFO selection process disclosed by Bouchard.

The motivation for the combination as taught by paragraph 29, pages 2-3 of the Bouchard is to use FIFOs as request queues in the memory banks conflict avoidance mode of operation.

Therefore, it would have been obvious to combine disclosures by Bouchard with teaching of Moore and Sherlock to obtain the invention as specified in the claim.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock in view of U.S. Patent No 5,557,750 to Moore et al. (hereinafter Moore).

3. *In regard to claim 1, Sherlock teaches*:

"a data buffering unit," **(e.g., see column 5, lines 46 and 52-53; Fig. 4).** *The First-In-First-Out (FIFO) Buffer System 400 shown in Fig. 4 represents the data buffering unit recited in the claim.*

"comprising:"

"a memory **(e.g., see element 100 in Fig. 13)** that stores data from a data transmitting device;" **(e.g., see column 11, lines 48-54; elements 1308 and 100 in Fig. 13).** *The System Bus Interface 1308 represents the transmitting device. However, Sherlock does not expressly teach:* "a memory read manager that prepares data stored in the memory for output prior to receiving a request for the data from a data reading device."

Moore teaches: "a memory read manager **(e.g., see element 128 in Fig. 1)** that prepares data stored in the memory for output prior to receiving a request for the data from a data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5;**

element 135 in Fig. 1) *for prefetching the FIFO data and storing it into a prefetch register for outputting to the host prior to the host request.*

Disclosures by Moore and Sherlock are analogous because both references teach methods of managing FIFO memory.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Sherlock to include the FIFO prefetching disclosed by Moore.

The motivation for prefetching data as taught by column 2, lines 4-7 of the Moore to allow data to be available when the host request it, eliminating host waiting for an internal data bus cycle. By thus eliminating host waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to combine teaching of Moore with Sherlock to obtain the invention as specified in the claim.

4. In regard to claim 2, Sherlock teaches:

" Wherein the memory comprises a plurality of first- in-first-out (FIFO) memories." **(e.g., see column 11, line 52; element 100 in Fig. 13).** *The Memory 100 shown in Fig. 13 contains multiple logical FIFOs.*

5. In regard to claim 3, Sherlock teaches:

"wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories." **(e.g., see column 11, lines 57-65; elements 100 and 1325 in Fig. 13).** *The Dequeue Control and Empty Indicator*

(element 1325 represents the memory read manage and provides READ (e.g., read enable) to the Memory 100.

6. *In regard to claim 4, Sherlock teaches*:

"wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit." **(e.g., see column 8, lines 36-64; element 414 in Fig. 4).** *For example the Next Read Register File stores the pointer or address for the next logical FIFO to be selected.*

7. *In regard to claim 5, Sherlock teaches*:

"wherein the memory read manager comprises a read selector, coupled to data outputs of each of the FIFO memories **(e.g., see element 414 in Fig. 4; element 706 in Fig. 7)**, that selects an appropriate data output to receive data from in response to a read address from the data reading device." **(e.g., see column 6, lines 44-59; Fig. 7).** *Element 706 shown in Fig. 7 is a n:1 mux or selector that select one of register (e.g., logical FIFO) within the Register File 700.*

8. *In regard to claim 6, Sherlock teaches*:

"wherein the memory read manager comprises a plurality of read pointer managers **(e.g., see column 5, lines 55-56)**, each corresponding to one of the FIFO memories," **(e.g., see column 8, lines 38-40)**. *However, Sherlock does not expressly teach:*

"the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device."

Moore teaches: "the read pointer managers **(e.g., see element 128 in Fig. 1)** transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1).** *The motivation for combining the two references is based on the same rational given in claim 1.*

Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock in view of Moore as applied to claim 2 above, and further in view Bouchard.

9. *In regard to claim 7, Sherlock teaches*:

"comprising a memory write manager **(e.g., see element 1324 in Fig. 13)** that directs data from the data transmitting device **(e.g., see element 1308 in Fig. 13)** to be written into each of the FIFO memories," **(e.g., see column 12, lines 5-7; element 100 in Fig. 13).** *However neither Sherlock nor Moore teaches:* "in a round robin fashion."

Bouchard teaches "in a round robin fashion." **(e.g., see paragraph 33 in page 3)** *for selecting the FIFO queues for the access requests in accordance to round-robin selection process.*

Disclosures by Bouchard, Moore, and Sherlock are analogous since all references teach managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the combined teaching of Moore and Sherlock to include the round-robin FIFO selection disclosed by Bouchard.

The motivation for combination as taught by paragraph 29, pages 2-3 of the Bouchard is to use a round-robin selection process for selecting a FIFO from a plurality of FIFOs to avoid memory access conflict.

Therefore, it would have been obvious to combine disclosures by Bouchard with teaching of Moore and Sherlock to obtain the invention as specified in the claim.

10. In regard to claim 10, Sherlock teaches:

"wherein the memory write manager **(e.g., see element 1324 in Fig. 13)** comprises a write selector that transmits a write enable signal and data from the data transmitting device to an appropriate FIFO memory in response to the work address manager." **(e.g., see column 11, lines 53-56).**

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock in view of Moore and U.S. Patent No. 6,891,397 B1 to Brebner.

11. In regard to claim 11, *Sherlock teaches:*

"memory blocks that form comprises a plurality of first-in-first-out (F1FO) memories that store data from a data transmitting device;" **(e.g., see column 11, lines 48-54; elements 1308 and 100 in Fig. 13).** *The element 100 represents the memory blocks and element 1308 represents the transmitting device recited in the claim. However, Sherlock does not teach:* "logic elements that form a memory read manager that

prepares data stored in the FIFO memories for output prior to receiving a request for the data from a data reading device; A programmable logic device (PLD),"

Moore teaches: "a memory read manager that prepares data stored in the FIFO memories for output prior to receiving a request for the data from a data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1).**

Brebner teaches: "A programmable logic device (PLD)," **(e.g., see column 2, lines 22-24; column 7, lines 44-46; elements 326-1 to 326-4)** *for using PLD to implement logic and memory functions including FIFO buffers.*

Disclosures by Sherlock, Moore, and Brebner are analogous because all references teach methods of implementing and managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to include the PLD system disclosed by Berbner and the prefetch/restore mechanism taught by Moore to implement the bus bridge taught by Sherlock.

The motivation for including PLD as taught by column 1, lines 36-37 of the Brebner is to implement a system-level integration for flexibility and efficiency. Furthermore, the motivation for including the prefetch/restore mechanism as taught by column 2, lines 4-7 of the Moore is to allow data to be available when the host request it, eliminating host waiting for an internal data bus cycle. By thus eliminating host waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to include teachings of Brebner and Moore to Sherlock to obtain the invention as specified in the claim.

12. *In regard to claim 12, Sherlock teaches*:

"wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories." **(e.g., see column 11, lines 57-65; elements 100 and 1325 in Fig. 13).**

13. *In regard to claim 13, Sherlock teaches*:

"wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit." **(e.g., see column 8, lines 36-64; element 414 in Fig. 4).**

14. *In regard to claim 14, Sherlock teaches*:

"wherein the memory read manager comprises a read selector coupled to data outputs of each of the FIFO memories **(e.g., see element 414 in Fig. 4; element 706 in Fig. 7)**, that selects an appropriate data output to receive data from in response to a read address from the data reading device." **(e.g., see column 6, lines 44-59; Fig. 7).**

15. *In regard to claim 15, Sherlock teaches*:

"wherein the memory read manager comprises a plurality of read pointer managers **(e.g., see column 5, lines 55-56)**, each corresponding to one of the FIFO memories," **(e.g., see column 8, lines 38-40)**. *However, Sherlock does not expressly teach:*

"the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device."

Moore teaches: "the read pointer managers **(e.g., see element 128 in Fig. 1)** transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1).** *The motivation for combining the two references is based on the same rational given in claim 1.*

ALLOWABLE SUBJECT MATTER

Claims 8-9 and 17-21 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claim 8 in instant application is the combination with the inclusion of the following limitations: **wherein the memory write manager comprises a write address manager that determines which of the FIFO memories to access in response to a write address received from the data transmitting device.**

2. The primary reason for allowance of claim 9 in instant application is the combination with the inclusion of the following limitations: **wherein the write address manager determines a write address in one of the FIFO memories to write data in response to the write address received from the data transmitting device.**

3. The primary reason for allowance of claim 17 in instant application is the combination with the inclusion of the following limitations: ***wherein the first data was***

prepared for output by the first FIFO memory prior to a generation of the read address from the data reading device.

4. The primary reason for allowance of claim 18 in instant application is the combination with the inclusion of the following limitations: **wherein the first data is output within a clock cycle after the first read address from the data reading device is generated.**

5. The primary reason for allowance of claim 19 in instant application is the combination with the inclusion of the following limitations: **wherein preparing the next data from the next storage element from the first FIFO memory to output comprises transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.**

6. The primary reason for allowance of claims 20-21 in instant application is the combination with the inclusion of the following limitations: **selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract***

should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 5,210,749 to Firoozmand describes Configuration of SRAMS as logical FIFOS for transmit and receive of packet data.

2. U. S. Patent No. 5,412,646 to Cyr *et al. describes Asynchronous transfer mode switch architecture.*

3. U. S. Patent No. 5,977,791 to Rubin et al. describes Embedded memory block with FIFO mode for programmable logic device.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information

for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

2005-11-11

DONALD SPARKS
SUPERVISORY PATENT EXAMINER